

CLAIMS

What is claimed is:

1. An apparatus comprising:

a signal layer including a first and a second signal trace;

5 a first reference plane including a first slot substantially parallel to the first and second signal traces; and

a dielectric layer having at least a first portion disposed between the signal layer and the first reference plane.

2. The apparatus of claim 1 wherein each of the first and second signal traces

10 comprise a first portion with a first width, and a second portion with a second width.

3. The apparatus of claim 2 wherein the first slot comprises a first portion and a second portion having a first slot width and a second slot width, respectively.

4. The apparatus of claim 3 wherein the first and second portions of the first slot correspond to the first and second portions, respectively, of the first and second

15 signal traces.

5. The apparatus of claim 3 wherein each of the first and second signal traces further comprises a third portion with a third width and the first slot comprises a third portion, comprising a third slot width, corresponding to the third portion of the first and second signal traces.

6. The apparatus of claim 1 wherein the first and second signal traces have a first and a second signal trace width wherein the first signal trace width is substantially the same as the second signal trace width.

7. The apparatus of claim 1 wherein the signal layer further includes a third and a
5 fourth pair of signal traces and a second slot.

8. The apparatus of claim 1 further comprising:

a second reference plane including a second slot substantially parallel to the
first and second signal traces; and

the dielectric layer further includes a second portion disposed between the
10 signal layer and the second reference plane.

9. An assembly comprising:

an apparatus comprising:

a signal layer including a first and second signal trace;

a first reference plane including a first slot substantially parallel to the first
15 and second signal traces; and

a dielectric layer having at least a first portion disposed between the signal
layer and the first reference plane;

a processor coupled to the apparatus; and

a networking interface coupled to the apparatus.

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10. The assembly of claim 9 wherein the first and second signal traces are coupled to the processor and the memory device.
11. The assembly of claim 9 wherein each of the first and second signal traces comprise a first portion with a first width and a second portion with a second width.
- 5 12. The assembly of claim 11 wherein the first slot comprises a first portion and a second portion having a first slot width and a second slot width, respectively.
13. The assembly of claim 12 wherein the first and second portions of the first slot correspond to the first and second portions, respectively, of the first and second signal traces.
- 10 14. The assembly of claim 9 further comprising:
a second reference plane including a second slot substantially parallel to the first and second signal traces; and
the dielectric layer further includes a second portion disposed between the signal layer and the second reference plane.
- 15 15. The assembly of claim 9 wherein the first and second signal trace are to facilitate propagation of a differential signal pair.
16. A system comprising:
an assembly comprising:
an apparatus comprising:

a signal layer including a first and second signal trace;
a first reference plane including a first slot substantially parallel to the
first and second signal traces; and
a dielectric layer having at least a first portion disposed between the
5 signal layer and the first reference plane; and
a processor coupled to the apparatus; and
a networking device coupled to the assembly.

17. The system of claim 16 wherein the a assembly further comprises a networking interface, wherein the networking interface is coupled to the networking device.

10 18. The system of claim 16 wherein the assembly further comprises an interface to persistent storage and wherein the system further comprises persistent storage coupled to the interface to persistent storage.

19. A method of routing circuit board traces comprising:

routing a first signal trace and a second signal trace substantially parallel to
15 the first signal trace on a signal plane of a circuit board; and
routing a slot in a reference plane of the circuit board substantially parallel to
the first second signal traces, for at least a portion of the first and second
signal traces.

20. The method of claim 19 wherein the substantially parallel portion of the first and
20 second signal traces comprises a first portion with a first width and a second portion with a second width.

21. The method of claim 20 wherein said routing of a slot comprises routing a first portion and a second portion of the slot, with a first and a second slot width respectively, corresponding to the first and second portions of the first and second signal traces.